

ISO7220M Dual-Channel Digital Isolator EVM

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1 Introduction

This user's guide details the evaluation module (EVM) operation of the factory installed ISO7220M dual-channel digital isolator. However, the EVM board may be reconfigured by a user for use with any of the ISO7220x or ISO7221x dual-channel isolators.

The EVM may be reconfigured for use with the ISO7220A, ISO7220B and ISO7220C same-channel direction isolators and the ISO7221A, ISO7221A, ISO7221C and ISO7221M opposing-channel direction isolators.

This guide also explains the user configurable I/O loads for both dual-channel isolator EVM configurations, and presents a typical lab setup with input and output waveforms.

1.1 Overview

The ISO7220x and ISO721x dual digital isolators have a logic input and output buffer separated by a silicon oxide (SiO₂) insulation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, and then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received for more than 4 μs, the input is assumed to be unpowered or not functional, and the failsafe circuit drives the output to a logic-high state.

CAUTION

Note that although these devices provide galvanic isolation of up to 4000 V, this EVM cannot be used for isolation voltage testing. It is designed for the examination of device operating parameters only and will be damaged if high voltage (> 5.5 V) is applied anywhere in the circuit.

1.2 Functional Configuration of the Dual-Channel Digital Isolator

The pin-outs of the dual-channel digital isolators are displayed in [Figure 1](#). The EVM comes with an ISO7220M installed; however, the user may reconfigure the EVM for use with any of the footprints.

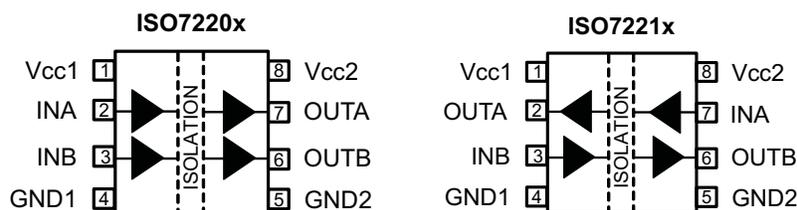


Figure 1. The ISO7220x and ISO7221x Pinouts

The ISO7220A, ISO7220B, ISO7220C, ISO7221A, ISO7221B and ISO7221C have TTL input thresholds and an input noise filter that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device.

The ISO7220M and ISO7221M have a CMOS Vcc/2 input threshold, but do not have the noise filter and the additional propagation delay.

1.3 The EVM Signal Paths of the ISO7220x and ISO7221x Isolators

This multifunctional EVM is designed with signal paths shown in Figure 1, Figure 2, and Figure 3 for the evaluation of the ISO7220x and ISO7221x dual-channel isolators.

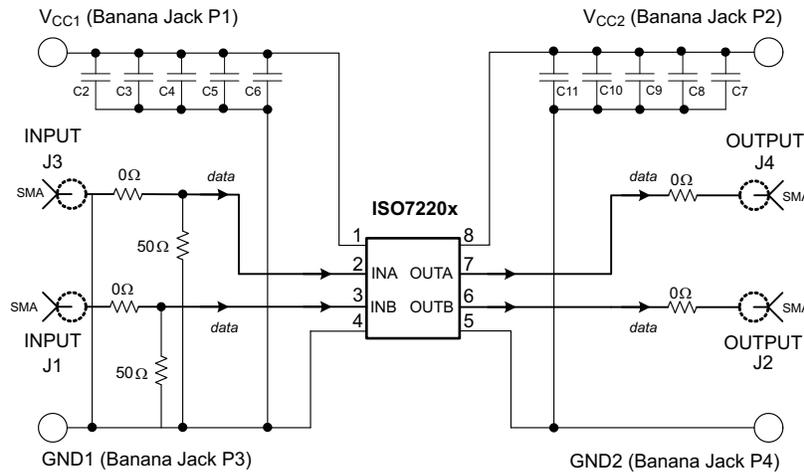
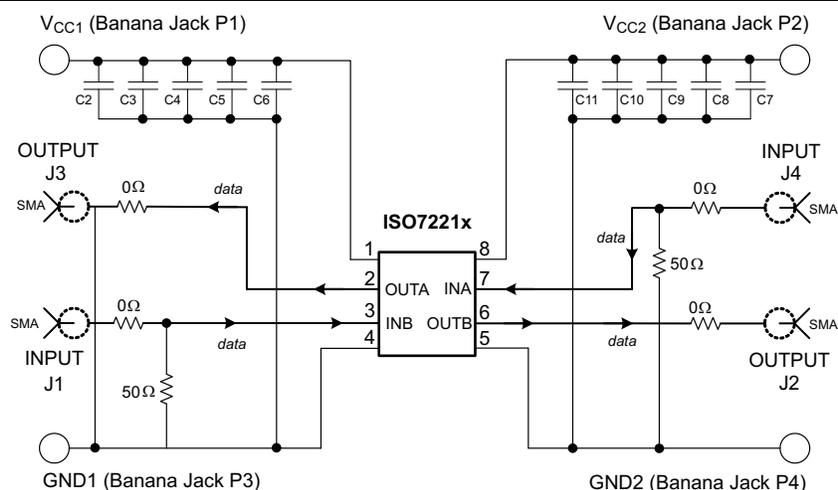


Figure 2. The ISO7220x Same-Channel Direction Schematic

Table 1. ISO7220x EVM Connections

Connection	Label	Description
J1		SMA connector to the INB input, pin 3
J2		SMA connector to the OUTB output, pin 6
J3		SMA connector to the INA input, pin 2
J4		SMA connector to the OUTA output, pin 7
P1	V _{CC1}	Input power supply banana jack
P2	V _{CC2}	Output power supply banana jack
P3	GND1	Input power ground connection banana jack
P4	GND2	Output power ground connection banana jack
JMP1		3-pin jumper V _{CC1} , input, GND1
JMP2		3-pin jumper (unused)
JMP3		3-pin jumper – V _{CC1} , input, GND1
JMP4		3-pin jumper (unused)


Figure 3. The ISO7221x Opposing-Channel Direction Schematic
Table 2. ISO7221x EVM Connections

Connection	Label	Description
J1		SMA connector to the INB input, pin 3
J2		SMA connector to the OUTB output, pin 6
J3		SMA connector to the OUTA output, pin 2
J4		SMA connector to the INA input, pin 7
P1	V _{CC1}	Input power supply banana jack
P2	V _{CC2}	Output power supply banana jack
P3	GND1	Input power ground connection banana jack
P4	GND2	Output power ground connection banana jack
JMP1		3-pin jumper V _{CC1} , input, GND1
JMP2		3-pin jumper (unused)
JMP3		3-pin jumper (unused)
JMP4		3-pin jumper V _{CC2} , input, GND2

1.4 The ISO7220x EVM Configuration

The ISO7220x EVM configuration has SMA connectors (J1 and J3) set up as the input to the INA (pin 2) and INB (pin 3) of the ISO7220M in [Figure 1](#) and [Figure 2](#). **R2** and **R8** are 0-Ω input series resistors shown in [Figure 4](#), and are located next to the J1 and J3 input connectors. **R1** and **R5** are 50-Ω resistors from each input to ground, and are located on the bottom of the board as shown in [Figure 5](#).

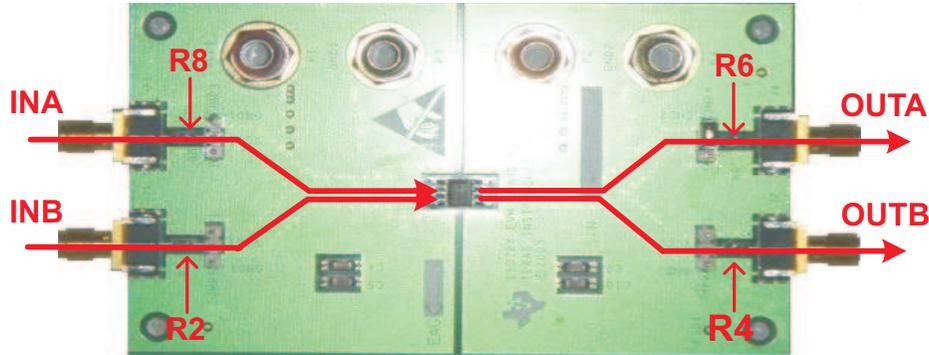


Figure 4. ISO7220x EVM, Top View

The output channel configuration of the ISO7220x EVM has the OUTA (pin 7) and OUTB (pin 6) of [Figure 1](#) and [Figure 2](#) connected to SMA connector (J2 and J4) through 0-Ω series resistor, **R4** and **R6**.

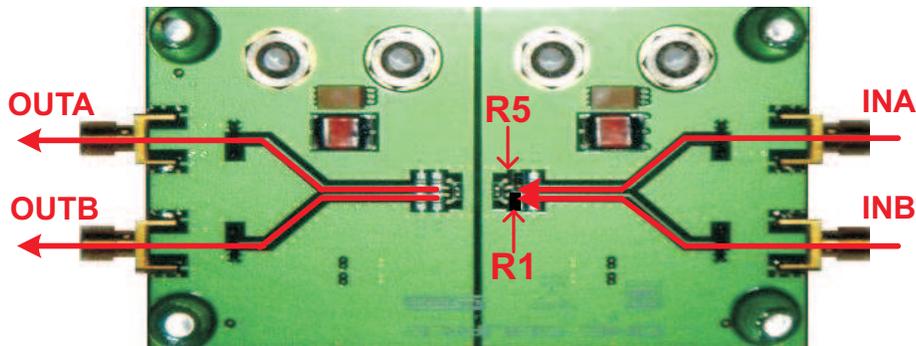


Figure 5. ISO7220x EVM, Bottom View

The pads for R3, R7, C1, C12, C13 and C14 are available on the bottom of the EVM for varied loading conditions if desired by a user.

1.5 The ISO7221x EVM Configuration

The ISO7221x EVM configuration has SMA connectors (J4 and J1) set up as the input to the INA (pin 7) and INB (pin 3) of the ISO7221x in [Figure 1](#) and [Figure 3](#). **R2** and **R6** are 0-Ω input series resistors shown in [Figure 6](#), and are located next to the J1 and J4 input connectors.

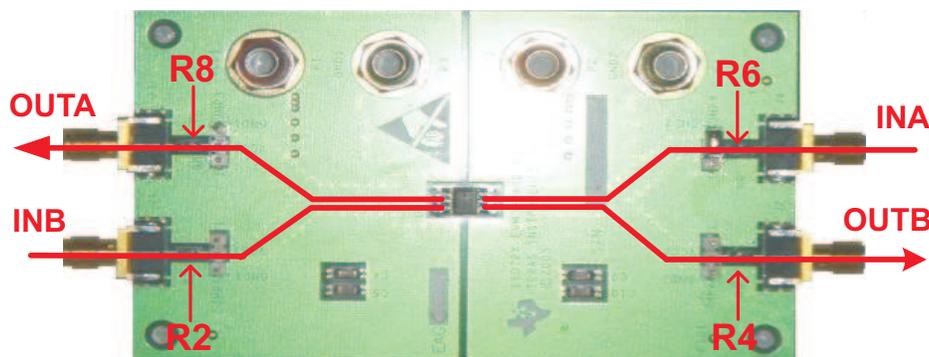


Figure 6. The ISO7221x EVM Top View

The output channel configuration of the ISO7221x EVM has the OUTA (pin 2) and OUTB (pin 6) of [Figure 1](#) and [Figure 3](#) connected to SMA connector (J3 and J2) through 0-Ω series resistor, **R8** and **R4**. **R1** and **R7** are 50-Ω resistors from each input to ground on the bottom of the board shown in [Figure 7](#).

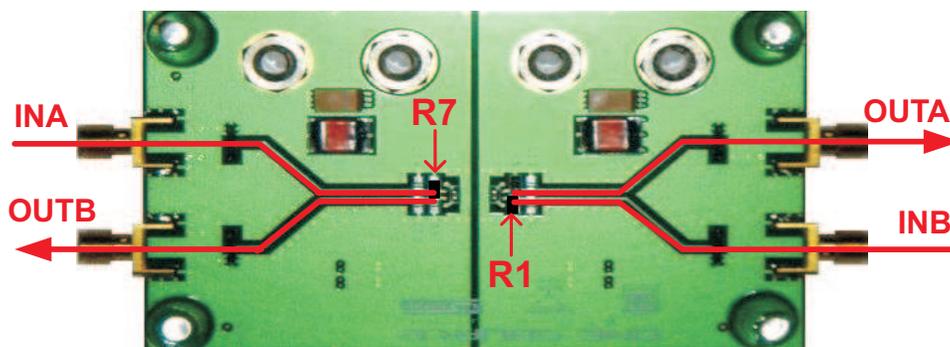


Figure 7. The ISO7221x EVM Bottom View

The pads for R3, R5, C1, C12, C13 and C14 are available on the bottom of the EVM for varied loading conditions if desired by a user.

2 EVM Setup and Operation

This section includes the setup and operation of the EVM for parameter performance evaluation. Typical waveforms are included.

2.1 Overview

The basic setup in [Figure 5](#) has the two power supplies required to evaluate isolator performance with 3.3-V on one side and 5-V on the other. If both sides are to be evaluated at the same supply voltage, only one power supply is required and can be used to power both sides of the EVM.

CAUTION

Note that this EVM is for operating parameter performance evaluation only and not designed for isolation voltage testing. Any voltage applied above the 5.5-V maximum recommended operating voltage of the digital isolators will damage the EVM.

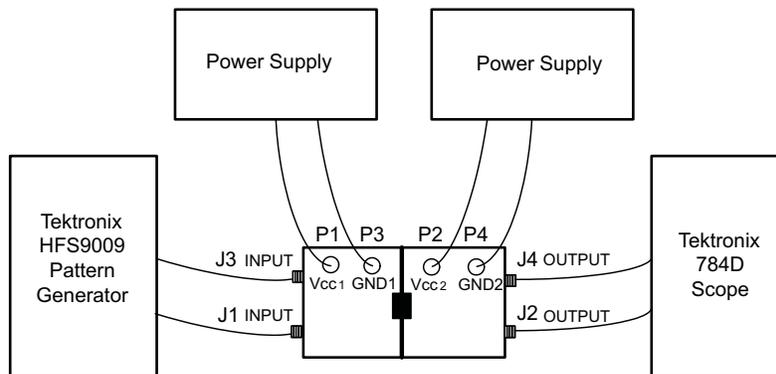


Figure 8. Basic EVM Operation

In [Figure 8](#), the J3 input to the EVM is a 20 MHz pulse displayed on channel 1 in [Figure 9](#). The J4 output of the EVM is channel 2.

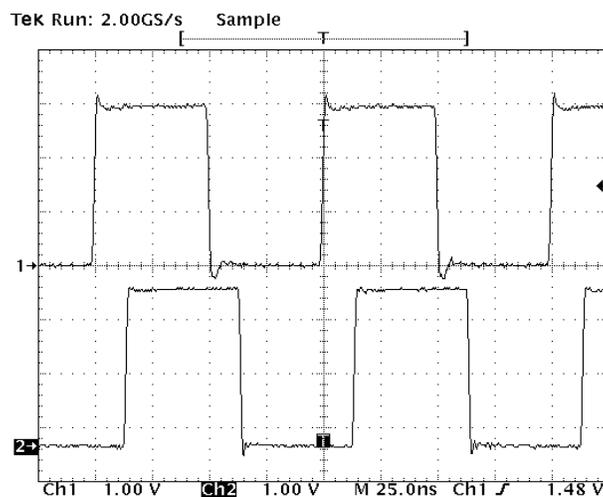


Figure 9. Typical Input and Output Waveforms

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 5.5 V and the output voltage range of 0 V to 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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